

BT8970H

Audio Player Microcontroller

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1 General Description

The BT897X is a low-power, highly integrated Bluetooth audio SoC tailored for TWS earphone applications. It adopts a 140MHz 32-bit RISC-V core with DSP and FPU extensions, integrating NOR on-chip Flash and 408KB RAM to support flexible GPIO control and fast program execution. Compliant with Bluetooth V6.0 (BR/EDR/BLE) with certified QDID, it supports stable TWS connection, master-slave switching and excellent RF receiving sensitivity. The chip integrates high performance dual ADC and dual DAC, supports mainstream Bluetooth audio protocols and full local audio decoding, and embeds comprehensive audio processing functions including ANC, ENC, AEC and PLC, together with NPU and programmable audio accelerators for high-quality audio performance. Equipped with abundant peripheral interfaces and a complete built-in PMU, it greatly reduces external components and BOM cost, serving as an optimal single-chip solution for high-performance TWS Bluetooth earphones.

SoC Architecture

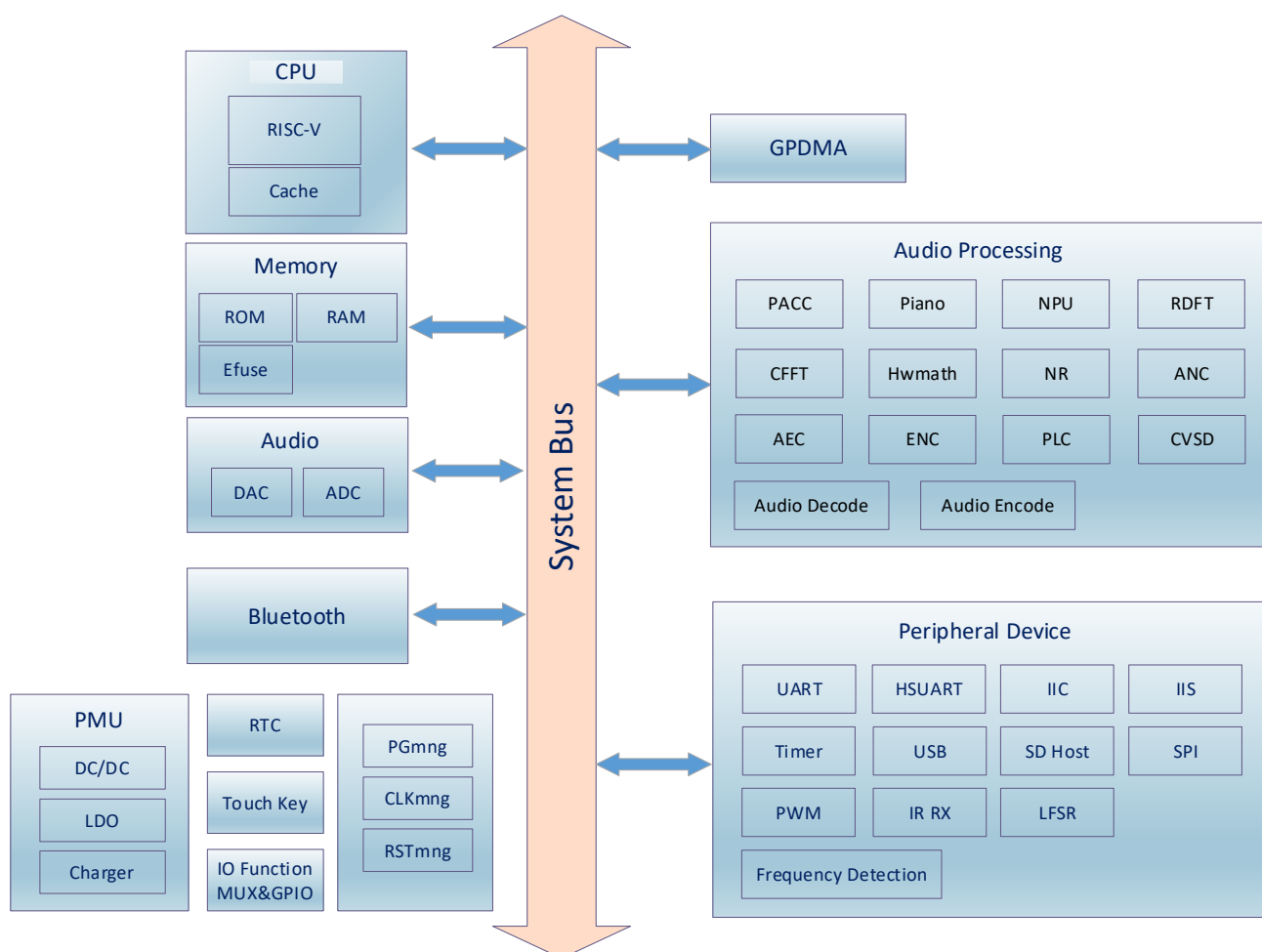


Figure 1-1 System Block Diagram

2 Product Features

CPU and Flexible IO

- High performance 32bit RISC-V processor Core with DSP instruction
- RISC-V contains floating point unit(FPU), supports floating point arithmetic
- RISC-V typical speed: 140MHz
- Program memory: internal 16Mbit flash
- Internal 408KB RAM for data and program
- Flexible GPIO pins with Programmable pull-up and pull-down resistors
- Support GPIO wakeup or interrupt

Bluetooth Radio

- Compliant with Bluetooth V6.0 + BR + EDR + BLE specification (QDID: Q380042)
- Bluetooth transmit power:
 - BR: up to 11dBm
 - EDR: up to 8dBm
- Bluetooth receiver sensitivity:
 - BR: -95.5dBm
 - EDR: -95dBm
 - BLE 1M: -99dBm
 - BLE 2M: -96dBm

Audio Interface

- High performance audio DAC x2:
 - SNR @VCM=0.9V: 122dB with DRE ON
 - SNR @VCM=0.9V: 112dB with DRE OFF
 - DNR @VCM=0.9V: 112dB
 - SNR @VCM=0.6V: 120dB with DRE ON
 - SNR @VCM=0.6V: 109dB with DRE OFF
 - DNR @VCM=0.6V: 109dB
 - Sample rate: 8KHz to 192 KHz
- High performance audio ADC x5:
 - SNR: 105dB
 - Sample rate: 8KHz to 384 KHz

- Support 5 channels single-ended or differential MIC amplifier input

Audio Processing

- support for SBC/AAC/LHDC/LDAC/LC3 Bluetooth audio transmission format
- support for mSBC wide band and LC3 super wide band speech coding
- support MP3/WAV/WMA/APE/FLAC/M4A audio decoding
- Acoustic echo cancellation/suppression (AEC, AES)
- Packet Loss Concealment(PLC) for voice processing
- Support far-end noise suppression (NR)
- Support 3 MIC DNN environment noise cancellation (ENC)
- Support Hybrid active noise cancellation (Hybrid ANC), adaptive ANC with environment noise detection and wind noise detection
- Support Neural network Processing Unit (NPU)
- Support Real Discrete Fourier Transform for NFFT=128/256/512/1024 (RDFT)
- Support complex FFT (CFFT)
- Two programmable accelerator (PACC) support a variety of filters, including FIR, BQ, DRC, frequency shifter and dynamics EQ

Peripheral and Interfaces

- 16-bit normal timer x 2; 32-bit normal timer x 3; multi-function 32-bit timer x 3
- Watch dog
- Full-duplex normal UART x 3; high speed UART with CTS/RTS x 1
- Master/Slave SPI x2
- Master/Slave IIS x1

- Master/Slave IIC x1
- IR receiver
- SD Card Host controller x 1
- Full speed USB 2.0 HOST/DEVICE controller x1
- 10-bit SARADC x 14ch
- Integrate IRTC
- Build in PMU, such as charger/buck/LDO

Applications

- Hybrid ANC Bluetooth headphones

Package

- QFN50 4*6

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

3 Power Management

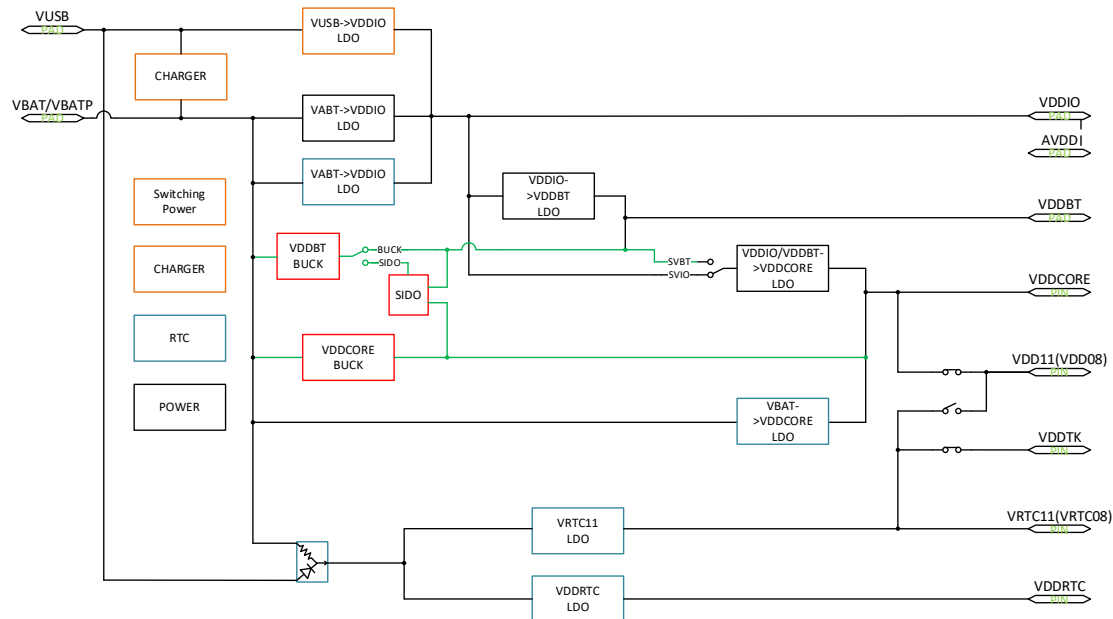


Figure 3-1 Power Path Diagram

BT897X integrates a Power Management Unit (PMU), which supports 3.0 V~4.5 V input from VBAT. The PMU includes multiple LDOs and DCDCs to achieve low power consumption.

PMU also integrates a battery charger. The lithium-ion battery charger features three stages: activation current mode (for activating low-charge batteries/low-voltage protection), trickle current mode (for recovering over-discharged battery capacity), startup mode (to ensure system startup power supply), constant current mode (for powering the system), follow mode, and constant voltage mode (to safely reach full capacity). The charger provides comprehensive safety features such as high input voltage protection and thermal regulation.

BT897X offers a variety of low-power features to reduce power consumption. It supports the following modes: power-down mode for individual peripherals and sleep mode for the processor. In addition, the BT897X is fabricated using an advanced low-leakage CMOS process to provide an ultra-low-leakage solution.

The BT897X provides the following LDOs:

VDDIO LDO generates a 2.3 V ~ 3.6 V (0.1 V/step) power rail for memory, codec, and GPIO.

VDDBT LDO generates a 0.6 V ~ 2.15 V (0.05 V/step) power rail for analog modules.

VDDCORE LDO generates a 0.6 V ~ 0.9 V (0.025 V/step) power rail for the digital core.

The BT897X provides the following switching-mode DCDCs for low-power applications, delivering high efficiency from light load to heavy load:

VDDCORE BUCK generates a 0.6 V ~ 0.9 V (0.025 V/step) power rail for the digital core;

VDDBT BUCK generates a 0.6 V ~ 2.15 V (0.05 V/step) power rail for analog modules/digital core.

4 Clock Management

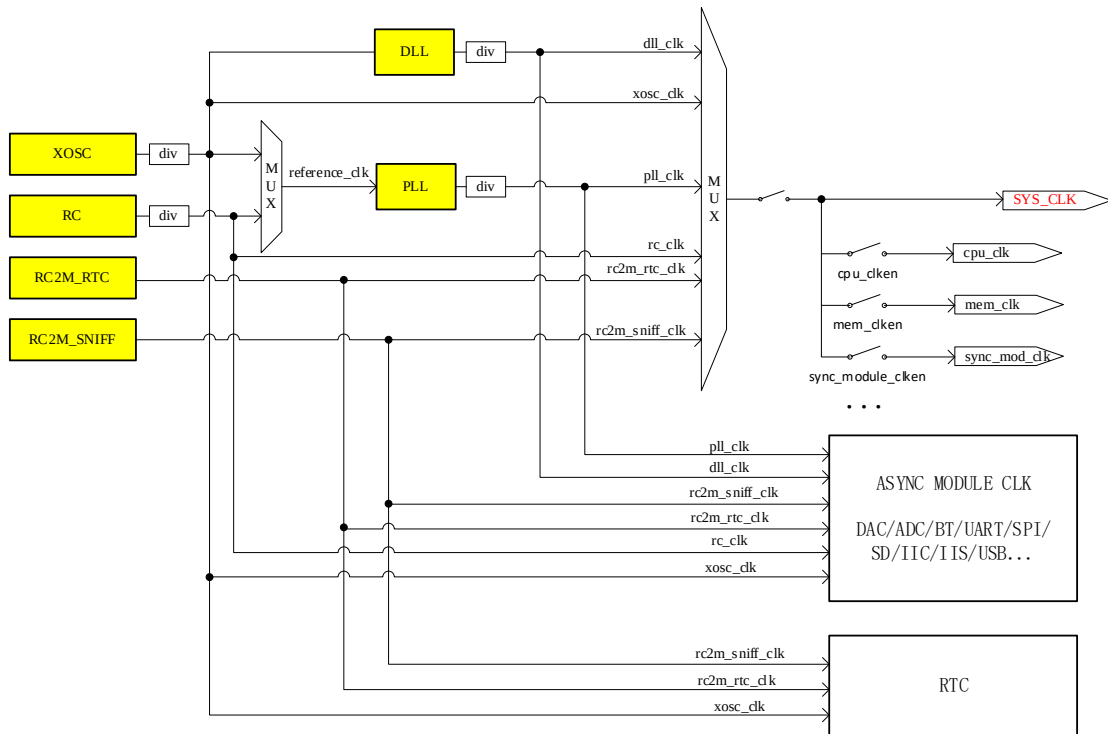


Figure 4-1 Clock System Diagram

4.1 Native Clock

BT897X features 4 native clock sources as follows:

- 1) **XOSC:** implemented by an internal active crystal oscillator circuit driving an external passive crystal. It primarily provides a 24MHz clock to the system, and also supports frequency-doubled and frequency-divided clocks to drive system operation.
- 2) **RC:** Internal RC oscillator. It mainly provides a 24 MHz clock and supports divided clocks for system operation. However, the RC clock frequency varies significantly with voltage and temperature.
- 3) **RC2M_RTC:** Derived from the dedicated RC oscillator in the PMU, with a typical frequency of 2 MHz. It primarily clocks the PMU and RTC modules, serves as the clock source for the WDT inside RTC, and supports low-power scenarios.
- 4) **RC_SNIFF** (typical 2 MHz): A low-temperature-drift and low-jitter RC clock, suitable for low-power applications requiring high stability.

4.2 Derived Clock

BT897X also features 2 derived clock sources:

- 1) Derived from the on-chip PLL, supporting multiple reference clock inputs. The PLL output frequency is adjustable and ranges from approximately 360 MHz to 550 MHz. It supports simultaneous output of the original frequency and divided clocks. Each clock has an independent enable bit. When a clock is not in use, software should disable the corresponding enable bit to prevent additional power

consumption.

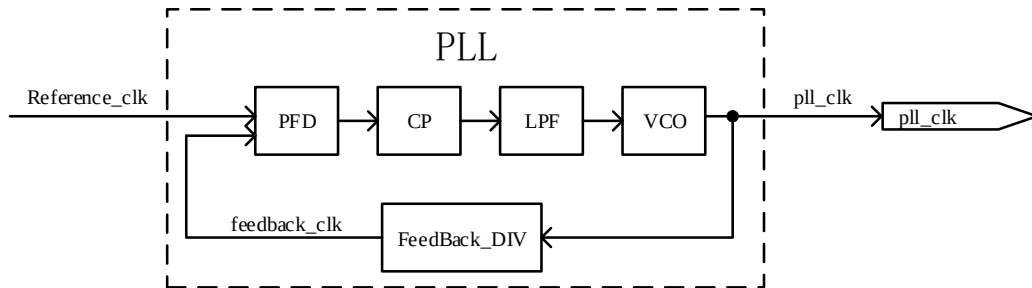


Figure 4-2 PLL Clock Source Schematic

- 2) Derived from the on-chip DLL, with a reference clock input. The DLL output range is an integer multiple of the reference clock, and the multiplication factor is adjustable. It supports simultaneous output of the original frequency and divided clocks. Each clock has an independent enable bit. When a clock is not in use, software should disable the corresponding enable bit to prevent additional power consumption.

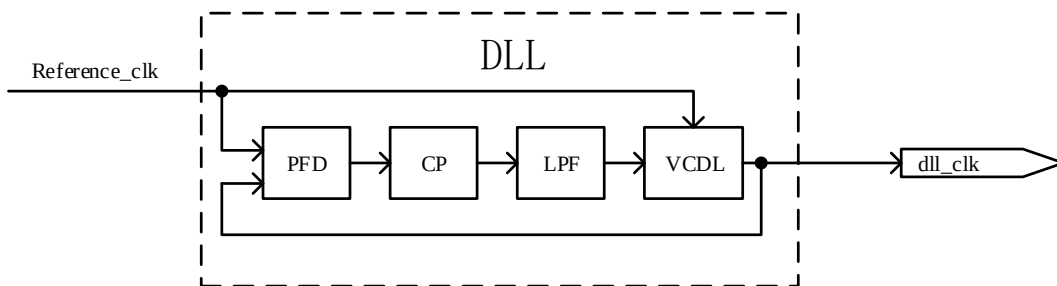


Figure 4-3 DLL Clock Source Schematic

5 Function Description

5.1 RISC-V Processor

The RISC-V processor has the following features:

- Up to 140 MHz clock frequency with 1.377 DMIPS/MHz (Dhrystone 2.1) and 2.212 Coremark/MHz (Coremark 1.0.1) performance
- Harvard architecture
- Full support for RV32IMC, BITMANIP, ZCB/ZCMP/ZCMT, ZFINX, PULP instruction set.
- Proprietary custom instruction set extensions: DSP (32-bit MAC, 64-bit adder), NEGSHIFT (signed bit shifting) and DIV64/32 (hardware division)
- Support for low priority and high priority (hp/hp2/hp3) interrupt
- Support 32KB Instruction/data software cache

5.2 Memory

BT897x supports internal and external memories.

- Embedded ROM 112KB for critical constants and code
- Embedded RAM 408KB for critical data and code
- SIP serial flash 4Mbit/8Mbit/16Mbit/32Mbit for custom programs

Refer to the [Product Feature](#) chapter for detailed Flash size specifications.

5.3 Bluetooth Subsystem

BT897X is fully compliant with Bluetooth BT/BLE 6.0 dual-mode. It also supports the LE Audio CIS/CIG and BIS/BIG full feature set.

BT897X supports the following Bluetooth radio features:

- Integrated Bluetooth TX/RX switch
- Fully integrated RF synthesizer without any external component

5.4 Audio Codec Subsystem

5.4.1 Overview

BT897X integrates an audio codec subsystem, which consists of the following blocks:

- 5x 24-bit high-quality ADCs with sample rates from 8 kHz to 384 kHz
- 2x 24-bit high-quality DAC with sample rates from 8 kHz to 192 kHz
- 2-channel AUX single-ended inputs
- 1x configurable I2S interface

The actual number of peripherals and channels varies by package. Refer to [product features](#) for detailed counts.

5.4.2 ADC

Supports line-level input and AC-coupled microphone input. Each analog input channel can be configured in differential, differential, or single-ended mode. In differential or differential mode, unused input pins shall be AC-coupled to ground. Each ADC adopts a 3rd-order Sigma-Delta converter. All ADCs are independent channels with identical functions. Each channel incorporates two gain stages: one analog gain stage and one digital gain stage.

For more information about the ADC parameters, refer to [Audio ADC Parameters](#).

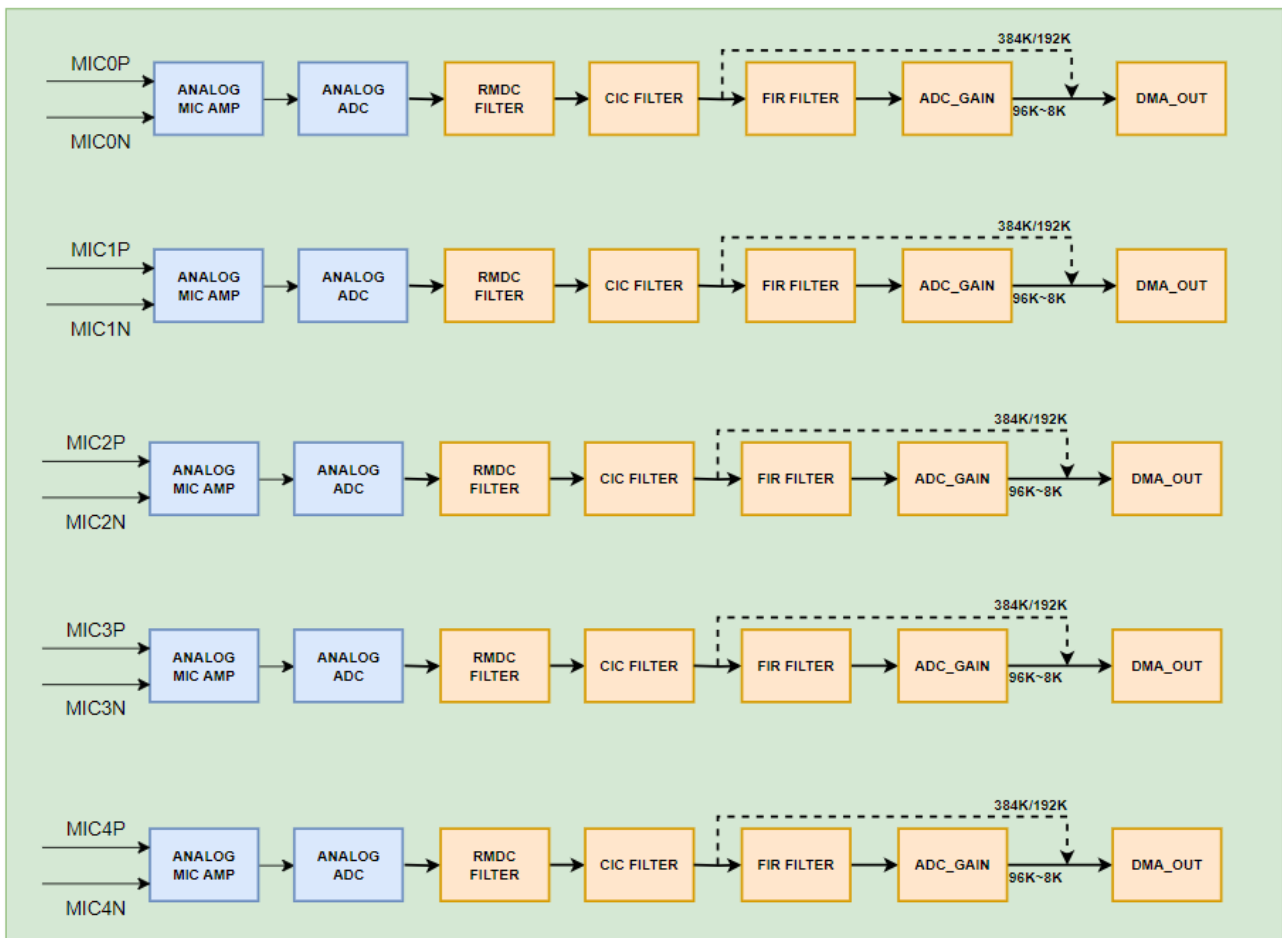


Figure 5-1 Analog-to-Digital Converter Diagram

5.4.3 DAC

Data can be routed to the output DAC path from the serial port, ADC and digital microphones. The analog output pins are capable of driving headphones or receiver speakers, and are biased at the common-mode (CM) voltage.

For more information about the DAC parameters, refer to [Audio DAC Parameters](#)

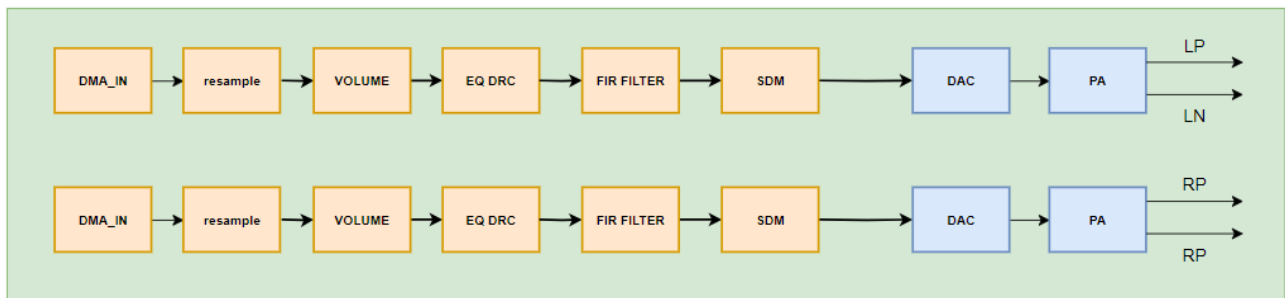


Figure 5-2 Digital-to-Analog Converter Diagram

5.5 System Peripherals

5.5.1 Crystal Oscillator

The BT897X integrates a 24MHz crystal oscillator circuit and built-in capacitors.

- Integrated 24MHz crystal oscillator circuit providing stable and reliable system clock;
- Built-in capacitors, with clock frequency offset adjustable during mass production;
- Flexible support for external capacitors.

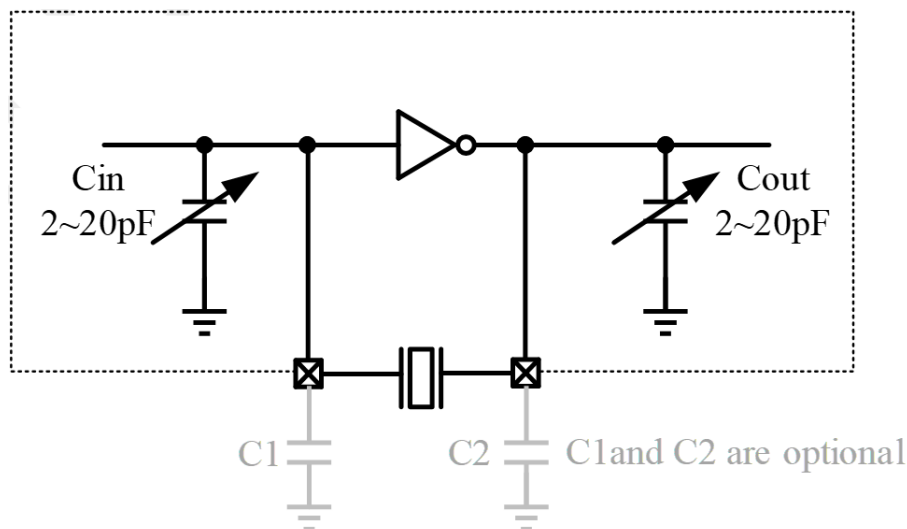


Figure 5-3 Crystal Oscillator

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_{IN} \times C_{OUT}}{C_{IN} + C_{OUT}} + C_{parasitic}$$

5.5.2 GPIO

BT897X provides programmable GPIOs, which support the following features:

- Direction and outputs of the IOs can be programmed separately.
- Input data of the IOs can be read back through memory-mapped registers.
- Support interrupts. The interrupt feature can be programmed separately.
- Support optional debounce for interrupts

5.5.3 Timer

- Timer0/1/2: support 32bit Timer-mode and Counter-mode
- Timer3/4: support 32bit Timer-mode, Counter-mode, Capture-mode.
- Timer5: support 32bit Timer-mode, Counter-mode, Capture-mode and PWM mode.

5.5.4 UART

- UART is a serial port capable of asynchronous transmission.
- The UART can function in full duplex mode.
- Equipped with 8-byte RX FIFO and 8-byte TX FIFO.

5.5.5 SPI

The SPI module supports multiple modes:

- General 3 wire mode: 1-bit clock in/out, 1-bit data output, 1-bit data input
- 2 wire mode: 1-bit clock in/out, 1-bit data output or input
- 2 data bus mode: 1-bit clock in/out, 2-bit data output or input
- 4 data bus mode: 1-bit clock in/out, 4-bit data output or input

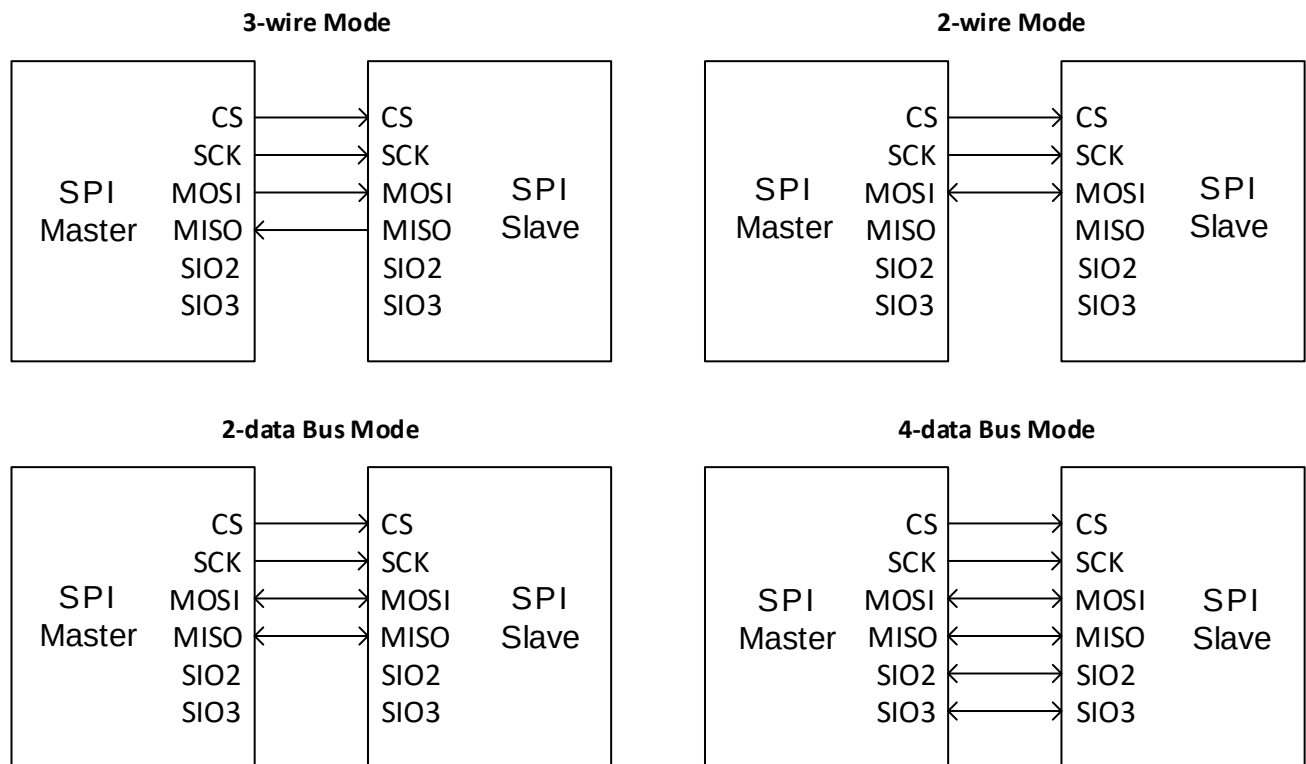


Figure 5-4 Pin connection between SPI master and SPI slave

5.5.6 IIC

- Support IIC single-master mode
- Support asynchronous clock source from RC2M or XOSC26M
- - Supports up to 4-bytes output data
- - Supports up to 4-bytes input data

- Support IIC done interrupt

5.5.7 IIS

- Support 44.1/48KHz sample rate
- Support output data source from SRC
- Support output data source from memory DMA
- Support input data DMA to memory
- Support IIS master mode 16/32bit data mode
- Support IIS slave mode
- Support IIS normal mode and left-justified mode
- Support PCM master mode
- Support DMA interrupt
- Support DMA address re-load

5.5.8 SARADC

The BT897X AUXADC features the following:

- 10-bit resolution
- Support 16 channels
- Maximum sample rate: 78k/s
- Maximum SARADC clock: 1MHz
- Integrated 100kΩ internal pull-up resistor

Note: The number of available channels is package-dependent. For the exact channel of each device, please refer to the [Product Features](#) section above.

5.5.9 Touch Key

The touch key controller performs key detection based on the effect of human body parasitic capacitance on the touch key capacitance. When a human finger touches the pin, the total external capacitance at the pin increases, which in turn increases the charge/discharge time of the capacitor. Detection is accomplished by measuring the difference in charge/discharge time, as shown in the figure below:

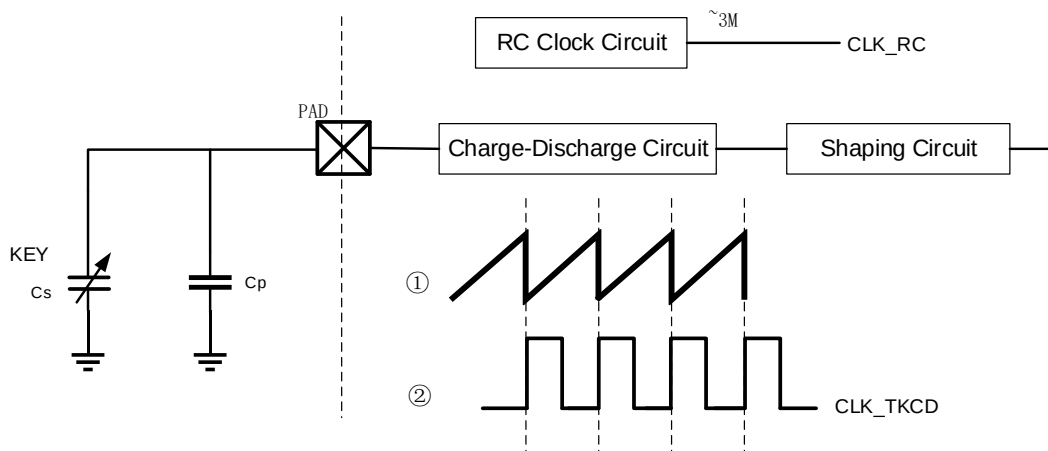


Figure 5-5 Capacitive Touch Schematic diagram

The chip internally includes the following circuits:

- Charge-discharge circuit
- Shaping circuit
- RC clock circuit

The charge-discharge circuit charges and discharges the capacitance at the external pin, corresponding to Waveform ①. The shaping circuit shapes Waveform ① to produce Waveform ②, which is then processed by the digital circuitry. By measuring the difference in charge/discharge time of Waveform ②, the chip determines whether a touch event has occurred.

5.5.10 PACC

The Programmable Accelerator (PACC) is a programmable hardware digital arithmetic acceleration module. It operates by placing the required operation module configurations, input/output buffers, and linked-list pointers in RAM according to a defined structure, and then starting the hardware via register writes. The PACC hardware then reads the configuration of the first module from RAM, fetches the input data, performs the corresponding operations, writes the results to the output buffer, and proceeds to the next module according to the linked list. After all modules have been processed, it notifies the software via interrupts or status registers, thereby reducing the software computational load. The PACC's processing chain is dynamically programmable, and multiple instances of the same operation module can be embedded, as long as the corresponding RAM space is allocated for each module.

The PACC supports the following operations: EQ (biquad IIR), DRC, MDRC, FIR and Dynamic EQ.

1. EQ (biquad IIR)

The EQ module is implemented using biquad IIR filters. It supports configurable band count and filter coefficients. The buffer length in RAM depends on the number of bands.

2. DRC / MDRC

The DRC module is used for dynamic gain control in audio, supporting 4-knee points and configurable attack and release time parameters. Built upon the EQ and DRC operations, it internally integrates an MDRC (multi-band DRC) module with configurable crossover frequencies.

3. FIR

The FIR module is used for digital signal FIR filter processing. It supports configurable filter order and filter coefficients.

4. Dynamic EQ

The Dynamic EQ module implements a dynamic equalization filter algorithm for audio. The dynamic EQ algorithm adaptively adjusts the gain of a filter at a certain frequency band based on the input signal amplitude. It supports configurable parameters such as center frequency, detection band, and amplitude threshold.

6 Package Definition

6.1 Pin Assignment

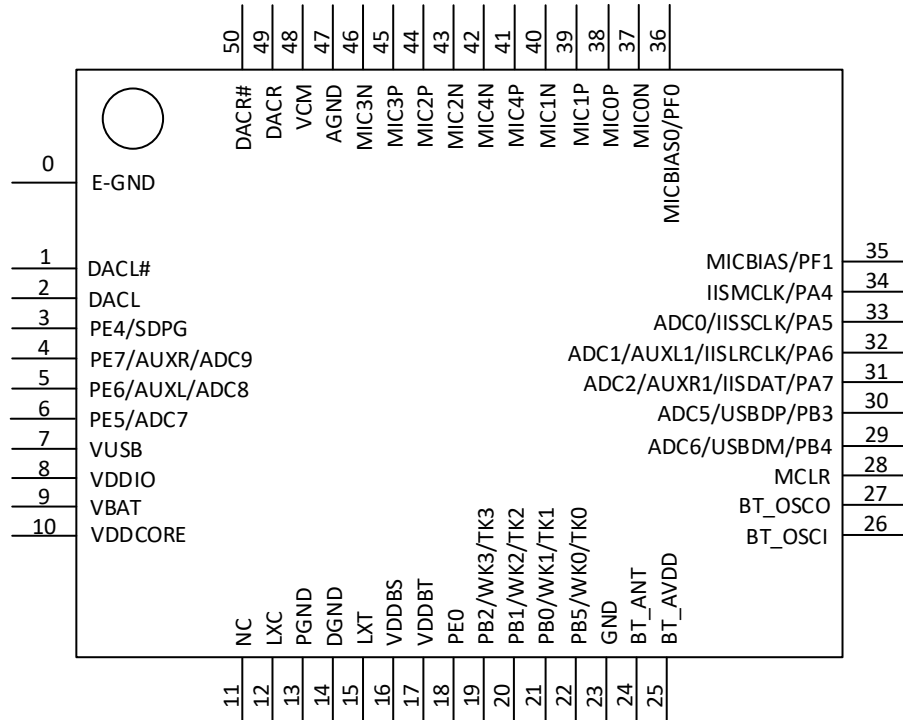


Figure 6-1 Pin Assignment

6.2 Pin Descriptions

Table 6-1 Pin Description

Pin No.	Name	Type	Drive(mA)	Function
0	E-GND	GND	/	E-pad
1	DACL#	A	/	DAC differential L#
2	DACL	A	/	DACL
3	PE4	I/O	8/32	SD PG IISMCLK-G2 INT1-G2 PWM5-G2 PE4
4	PE7	I/O	8/32	MICBIAS2-300R ADC9 AUXR0 SDDAT0-G3

				SPI1DO/SPI1DATA-G4 IISDO/DAT-G2 IIC_DAT-G5 TX0-G4 TX2-G1 HSTRX-G4 INT3-G1 PWM2-G3 TMR4CAP_G1/IR_G8 PE7
5	PE6	I/O	8/32	ADC8 AUXL0 SDCLK-G3 SPI1CLK-G4 IISLRCLK-G2 IIC_CLK-G5/G6 RX0-G4 RX2-G1 HSTRX-G9 INT2-G2 FMOSC-G6 PWM1-G3 TMR3CAP_G7/IR_G7 PE6
6	PE5	I/O	8/32	ADC7 SDCMD-G3 SPI1DI-G4/SPI2W_DIO1-G4 IISCLK-G2 IIC_DAT-G6 INT2-G1 FMOSC-G5 PWM0-G3 TMR3CAP_G6/IR_G6 PE5
7	VUSB	PWR	8	VUSB power input TX0-G6(RX) TX1-G3(RX) TX2-G3(RX)-Update HSTRX-G11
8	VDDIO	PWR	/	VDDIO power output
9	VBAT	PWR	/	VBAT power input
10	VDDCORE	PWR	/	VDDCORE power
11	NC	-	-	-
12	LXC	PWR	/	BUCK for VDDCORE
13	PGND	GND	/	Power ground
14	DGND	GND	/	Digital Ground
15	LXT	PWR	/	Buck for BT
16	VDDBS	A	/	SIDO input

17	VDDBT	PWR	/	BT power
18	PE0	I/O	8/32	IISDI-G2 TX0-G5(RX) INT1-G1 PWM4-G2 TMR3CAP_G5/IR_G5 PE0
19	PB2	I/O	8/32	Touch3 WK3 ADC4 SDDAT0-G2 SPI1DO/SPI1DATA-G3 IISDO/DAT-G3 IIC_DAT-G3 TX0-G2(RX) TX2-G2(RX) HSTRX-G2 INT2-G0 PWM0-G2 PB2
20	PB1	I/O	8/32	Touch2 WK2 ADC3 SDCLK-G2 SPI1CLK-G3 IISLRCLK-G3 IIC_CLK-G3/G4 RX0-G2 RX2-G2 HSTRX-G7 INT1-G0 FMOSC-G4 PWM5-G1 TMR3CAP_G4/IR_G4 PB1
21	PB0	I/O	8/32	Touch1 ADC11 SDCMD-G2 SPI1DI-G3/SPI2W_DIO1-G3 IISCLK-G3 IIC_DAT-G4 INT6-G0 FMOSC-G3 PWM4-G1

				TMR3CAP_G3/IR_G3 PB0
22	PB5	I/O	8/32	WK0 Main wakeup source 10S Reset Touch0 ADC12 SPI1DI-G1/SPI2W_DIO1-G1 IISDI-G3 INT5-G0 PWM3-G2 PB5
23	GND	GND	/	Ground
24	BT_ANT	A	/	BT ANT
25	BT_AVDD	PWR	/	BT RF Power
26	BT_OSCI	A	/	24M OSC input
27	BT_OSCO	A	/	24M OSC output
28	MCLR	A	/	Manual reset
29	PB4	I/O	8/32	USBDM ADC6 SDDAT0-G4/G6 SPI1DO/SPI1DATA-G1 IISMCLK-G3 IIC_DAT-G7 RX0-G3 HSTRX-G8 INT4-G0 FMOSC-G7 PWM2-G2 PB4
30	PB3	I/O	8/32	USBDP ADC5 SDDAT0-G5/SDCMD-G6 SPI1CLK-G1 IISDI-G1 IIC_CLK-G7 TX0-G3(RX)-Update HSTRX-G3 INT3-G0 PWM1-G2 PB3
31	PA7	I/O	8/32	Touch4

				ADC2 AUXR1 SDDAT0-G1 SPI1DO/SPI1DATA-G2 IISDO/DAT-G1 IIC_DAT-G1 TX0-G1 TX1-G1 HSTRX-G1 INT0-G0 PWM3-G1 PA7
32	PA6	I/O	8/32	Touch5 ADC1 AUXL1 SDCLK-G1/G4/G5/G6 SPI1CLK-G2 IISLCLK-G1 IIC_CLK-G1/G2 RX0-G1 RX1-G1 HSTRX-G6 INT0-G1 FMOSC-G2 PWM2-G1 TMR3CAP_G2/IR_G2 PA6
33	PA5	I/O	8/32	ADC0 SDCMD-G1/G4/G5 SPI1DI-G2/SPI2W_DIO1-G2 IISCLK-G1 IIC_DAT-G2 HSTRX RTS INT0-G2 FMOSC-G1 PWM1-G1 TMR3CAP_G1/IR_G1 PA5
34	PA4	I/O	8/32	IISMCLK-G1 HSTRX CTS INT0-G3 PWM0-G1 PA4
35	PF1	I/O	8/32	MICBIAS1-50R ADC13 IIC_DAT-G8 RX1-G2 HSTRX-G10 INT4-G1 PWM4-G3 PF1
36	PF0	I/O	8/32	MICBIAS0-50R ADC10 IIC_CLK-G8 TX1-G2(RX)

				HSTRX-G5 INT3-G2 PWM3-G3 TMR5CAP_G1/IR_G9 PF0
37	MIC0N	A	/	Microphone0 negative input
38	MIC0P	A	/	Microphone0 positive input
39	MIC1P	A	/	Microphone1 positive input
40	MIC1N	A	/	Microphone1 negative input
41	MIC4P	A	/	Microphone4 positive input
42	MIC4N	A	/	Microphone4 negative input
43	MIC2N	A	/	Microphone2 negative input
44	MIC2P	A	/	Microphone2 positive input
45	MIC3P	A	/	Microphone3 positive input
46	MIC3N	A	/	Microphone3 negative input
47	AGND	GND	/	Analog Ground
48	VCM	A	/	DAC VCM
49	DACR	A	/	DAC R
50	DACR#	A	/	DAC differential R#

Note: I/O: Digital input/output; I : Digital input; A : Analog Pin; PWR: Power Pin; GND: Ground.

7 Characteristics

7.1 PMU Parameters

Table 7-1 PMU voltage input Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VUSB	Charger Voltage input	4.6	5.0	5.5	V	
VBAT	Voltage input	3.0	3.7	4.5	V	

Table 7-2 VDDIO LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDIO	Voltage output	2.4	3.3	3.6	V	Light Loading condition Step 0.1v
Δ VDDIO	Output Mismatch 1-sigma	-	8.4	-	mV	VDDIO=3.3v
ILOAD	Maximum output current	-	-	150	mA	@VBAT=3.6v
ISC	Short Circuit Current Limit	-	-	120	mA	@VBAT=3.8v

Table 7-3 VDDBT LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDBT/BT_AVDD	Voltage output	0.6	1.35	2.15	V	Light Loading condition Step 0.05v
Δ VDDBT	Output Mismatch 1-sigma	-	9	-	mV	VDDBT=1.35v
ILOAD	Maximum output current	-	-	100	mA	@VBAT=3.0v
ISC	Short Circuit Current Limit	-	-	320	mA	@VBAT=3.8v

Table 7-4 VDDCORE LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDCORE	Voltage output		0.8		V	Light Loading condition Step 0.025v
Δ VDDCORE	Output Mismatch 1-sigma	-	4.3	-	mV	VDDCORE=0.8v
ILOAD	Maximum output current	-	-	30	mA	@VBAT=3.6v
ISC	Short Circuit Current Limit	-	-	300	mA	@VBAT=3.8v

Table 7-5 VDDBT BUCK Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDBT	Voltage output	0.6	1.35	2.15	V	Light Loading condition Step=0.05v
Δ VDDBT	Output Mismatch 1-sigma	-	6	-	mV	VDDBT=1.35v
ILOAD	Maximum output current	-	-	216	mA	@VBAT=3.8v
ISC	Short Circuit Current Limit	-	-	360	mA	@VBAT=3.8v

Table 7-6 VDDCORE BUCK Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDCORE	Voltage output		0.8		V	Light Loading condition Step=0.025v
Δ VDDCORE	Output Mismatch 1-sigma	-	5	-	mV	VDDCORE=0.8v
ILOAD	Maximum output current	-	-	216	mA	@VBAT=3.8v
ISC	Short Circuit Current Limit	-	-	360	mA	@VBAT=3.8v

Table 7-7 Battery Charge

Symbol	Parameter	Min	Typ	Max	Unit	Condition
VUSB	Charger input voltage	4.6	5.0	5.5	V	
VBAT _{float}	Charge Voltage	4.18	4.20	4.22	V	VUSB>4.6V
		4.33	4.35	4.37	V	VUSB>4.75V
		4.38	4.40	4.42	V	VUSB>4.8V
		4.43	4.45	4.47	V	VUSB>4.85V
I _{CH}	Charge current	5		320	mA	VBAT<=VBAT _{float} -150mV VUSB>=VBAT _{float} +550mV Step=5mA
I _{End}	End of charge current	2.5		37.5	mA	Step=2.5mA
V _{Trickle}	Trickle charge Voltage	2.9	3.0	3.1	V	VUSB>4.6V

7.2 IO Parameters

Table 7-8 I/O Parameters

GPIO—Electrical Characteristics							
Symbol	Description	Related GPIO	Min	Typical	Max	Units	Conditions
VIL	Low-level input voltage		-0.3		0.99	V	VDDIO=3.3V
VIH	High-level input voltage		2.31		3.6	V	VDDIO=3.3V
Driver Ability 1	Output Driver Ability 1			32		mA	VDDIO=3.3V
Driver Ability 0	Output Driver Ability 0			8		mA	VDDIO=3.3V
RPUP0	Internal pull-up resistor 0 resistance accuracy $\pm 25\%$		7.5	10	12.5	K Ω	
RPUP1	Internal pull-up resistor 1		0.225	0.3	0.375	K Ω	
RPUP2	Internal pull-up resistor 2		150	200	250	K Ω	
RPDN0	Internal pull-down resistor 0		7.5	10	12.5	K Ω	
RPDN1	Internal pull-down resistor 1		0.225	0.3	0.375	K Ω	
RPDN2	Internal pull-down resistor 2		150	200	250	K Ω	

Table 7-9 Internal Resistor Characteristics

Port	General Output	High Drive	Internal Pull-Up Resistor (Ω)	Internal Pull-Down Resistor (Ω)	Comment
PA4-PA7 PB0-PB5 PE0, PE4-PE7	8mA	32mA	300/10K/200K	300/10K/200K	Internal pull-up/pull-down resistance accuracy $\pm 25\%$

Port	General Output	High Drive	Internal Pull-Up Resistor (Ω)	Internal Pull-Down Resistor (Ω)	Comment
PF0-PF1 PG0-PG5					
VUSB	8mA	-	10K	10K	

7.3 Audio DAC Parameters

Table 7-10 Audio DAC Differential Mode Parameters @VCM=0.6V

Parameter	Conditions	load	Min	Typ	Max	Unit	
Resolution					24	Bits	
Fsample			8	/	192	KHz	
Output Level	Sin -1Khz; BW=20-20KHz; A-Weighted, Stereo, Fsample 48KHz	32R	/	750	/	mVrms	
		16R	/	650	/	mVrms	
SNR		32R	/	108.7	/	dB	
		16R	/	107.8	/	dB	
THD+N		32R	/	-90	/	dB	
		16R	/	-90	/	dB	
Noise Floor		32R	/	2.70	/	uVrms	
		16R	/	2.60	/	uVrms	
Output Level		Sin -1Khz; BW=20-20KHz; A-Weighted, Single channel Fsample 48KHz	32R	/	750	/	mVrms
			16R	/	650	/	mVrms
SNR	32R		/	108.7	/	dB	
	16R		/	107.8	/	dB	
THD+N	32R		/	-90	/	dB	
	16R		/	-90	/	dB	
Noise Floor	32R		/	2.70	/	uVrms	

Parameter	Conditions	load	Min	Typ	Max	Unit
		16R	/	2.60	/	uVrms
DNR	DRE OFF	32R	/	108.7	/	dB
SNR	DRE ON	32R	/	120	/	dB
DRE ON	DRE ON	32R	/	0.78	/	uVrms

Table 7-11 Audio DAC Differential Mode Parameters @VCM=0.9V

Parameter	Conditions	load	Min	Typ	Max	Unit	
Resolution					24	Bits	
Fsample			8	/	192	KHz	
Output Level	Sin -1Khz; BW=20-20KHz; A-Weighted, Stereo, Fsample 48KHz	32R	/	1000	/	mVrms	
		16R	/	800	/	mVrms	
SNR		32R	/	111.5	/	dB	
		16R	/	110.5	/	dB	
THD+N		32R	/	-90	/	dB	
		16R	/	-90	/	dB	
Noise Floor		32R	/	2.70	/	uVrms	
		16R	/	2.60	/	uVrms	
Output Level		Sin -1Khz; BW=20-20KHz; A-Weighted, Single channel Fsample 48KHz	32R	/	1000	/	mVrms
			16R	/	880	/	mVrms
SNR	32R		/	111.5	/	dB	
	16R		/	110.5	/	dB	
THD+N	32R		/	-90	/	dB	
	16R		/	-90	/	dB	

Parameter	Conditions	load	Min	Typ	Max	Unit
Noise Floor		32R	/	2.70	/	uVrms
		16R	/	2.60	/	uVrms
DNR	DRE OFF	32R	/	111.5	/	dB
SNR	DRE ON	32R	/	122	/	dB
DRE ON	DRE ON	32R	/	0.78	/	uVrms

7.4 Audio ADC Parameters

Table 7-12 Audio ADC Parameters

Mode	Sym	Characteristics	Min	Typ	Max	Unit	Conditions
ADC Single-ended Mode	Gain			6		dB	VCM cap=1uF Input -4dBV @ Fin=1KHz Gain = 6dB
	SNR			103		dB	
	THD+N			-74		dB	
	Input Range	Maximum input voltage		-4		dBV	
ADC Differential Mode	Gain			6		dB	VCM cap=1uF Differential input Input -4dBV @ Fin=1KHz Gain=6dB
	SNR			105		dB	
	THD+N			-90		dB	
	Input Range	Maximum input voltage		-4		dBV	

7.5 BT Parameters

Table 7-13 BT Parameters

Characteristics	Min	Typical	Max	Unit	Conditions
Transmit Power@ Basic Rate		11		dBm	
Transmit Power@ EDR		8		dBm	

Characteristics	Min	Typical	Max	Unit	Conditions
RMS DEVM		9.5		%	Maximum TX power 2-DH5 packet
Peak DEVM		20		%	
EDR Relative Transmit Power		-3		dB	
Sensitivity @ Basic Rate		-95.5		dBm	BER=0.1%, using DH1 packet
Sensitivity @ EDR		-95		dBm	BER=0.01%, using 2-DH5 packet
Sensitivity @ 1M BLE		-99		dBm	PER=30.8%, 37byte
Sensitivity @ 2M BLE		-96		dBm	PER=30.8%, 37byte

7.6 Current Parameters

Table 7-14 Current Parameters

Symbol	Description	Min	Typ	Max	Unit	Conditions
Phone call	ESCO 2EV3		TBC		mA	The DCDC mode And VBAT =3.8v Without 16R/32R Speaker
Single-ear Play audio	AAC		TBC		mA	
Master of TWS Play audio	AAC		TBC		uA	
Slave of TWS Play audio	AAC		TBC		uA	
Power Off	Soft Power Off		TBC		uA	
Current Mute			TBC		uA	
Current Idle			TBC		uA	

7.7 Electrostatic Discharge Ratings

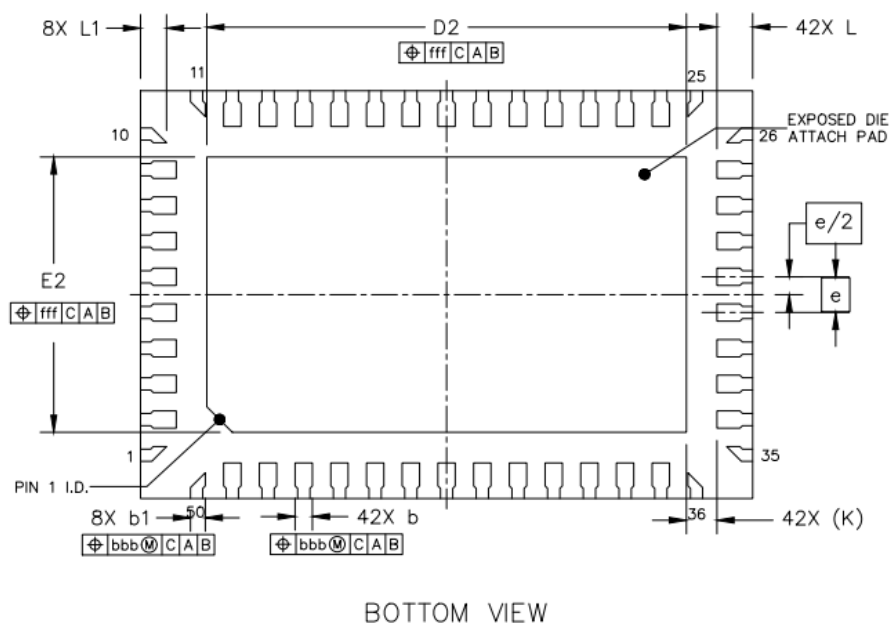
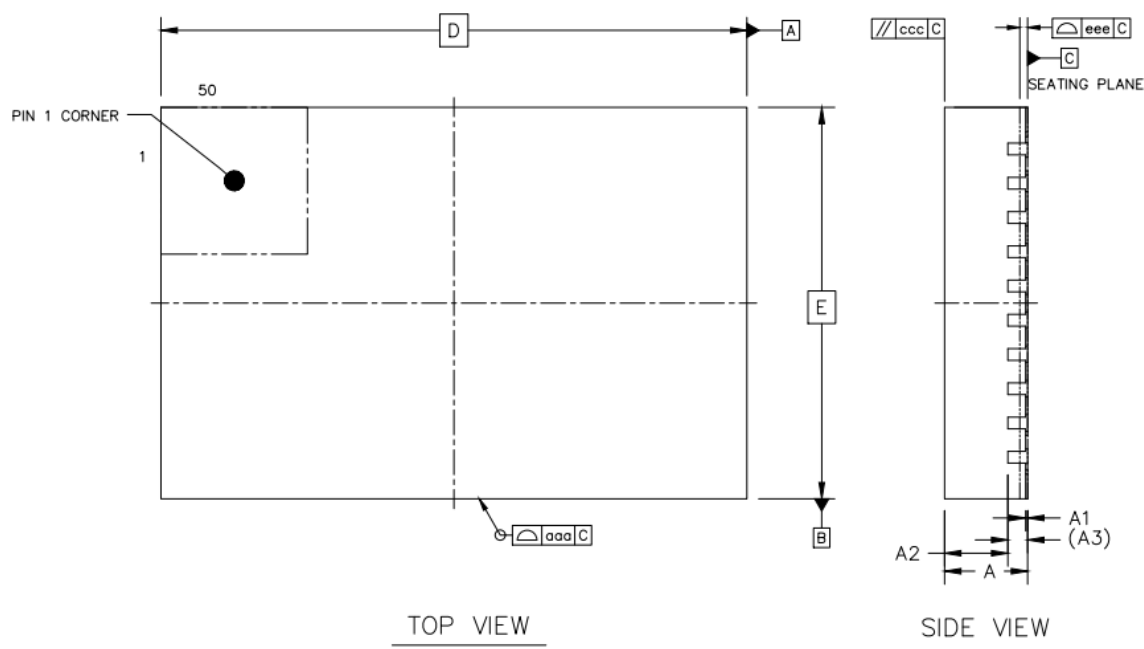
Table 7-15 ESD Electrical Characteristic

Parameter	Pin name	Typ.	Reference standard
Human body model(HBM)	All pins	±4KV	Mil-Std-883C Method 3015.9
Charged device model(CDM)	All pins	±1KV	JS-002
Latch up	All GPIO pins	±400mA	JESD78E
	All power pins	1.5x Vop max	

Note: 1.5x Vopmax=1.5 times maximum operating voltage.

All power pins=VBAT pin

8 Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.12	0.17	0.22
		b1	0.095	0.145	0.195
BODY SIZE	X	D	6 BSC		
	Y	E	4 BSC		
LEAD PITCH		e	0.35 BSC		
EP SIZE	X	D2	4.6	4.7	4.8
	Y	E2	2.6	2.7	2.8
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.15	0.25	0.35
LEAD TIP TO EXPOSED PAD EDGE		K	0.3 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.07		
EXPOSED PAD OFFSET		fff	0.1		

9 Tape and Reel Information

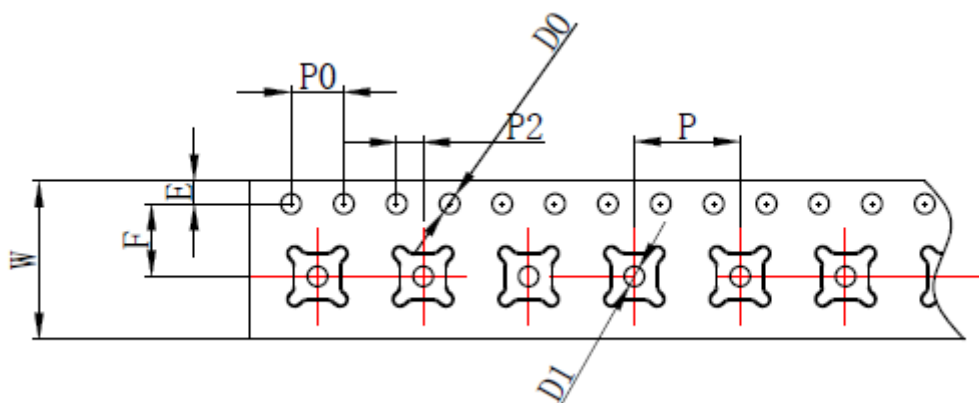


Figure 9-1 Tape Dimensions

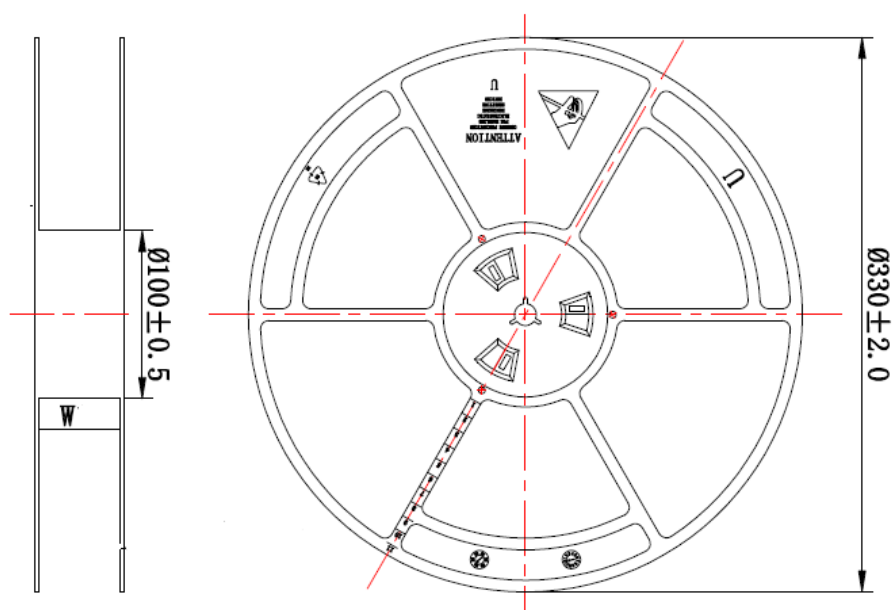


Figure 9-2 Reel Dimensions

Table 9-1 Tape and Reel Dimensions

Package Code	Number of Pins	Body Size (mm ²)	Package Pitch: P(mm)	Hold Pitch: P0 (mm)	Reel Diameter (mm)	Reel Width (mm)
QFN50	50	4*6	8	4	330	16



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